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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Garg *et al.*

Appl. No. 08/990,414

Filed: December 15, 1997

For: **SUPERSCALAR RISC INSTRUCTIONS SCHEDULING**

Art Unit: 2783

Examiner: Donaghue, L.

Atty. Docket: SP035.C3

Information Disclosure Statement Under 37 C.F.R. § 1.97(i)

Assistant Commissioner for Patents
Washington, D.C. 20231

Attn: Box Issue Fee
Batch No. Q76

Sir:

It is respectfully requested that this Information Disclosure Statement be placed in the file of the above-captioned application, for which Notification of Allowance has been received, in accordance with 37 C.F.R. § 1.97(i). Listed on accompanying Form PTO-1449 are documents for which a copy is provided. Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Brian S. Rosenbloom
Attorney for Applicants
Registration No. 41,276

Date: 5/26/1999

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FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
SP035.C3	08/990,414
APPLICANT: Garg *et al.*	
FILING DATE: December 15, 1997	GROUP: 2783

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	4,626,989	12/1986	Torii	364	200	
	AB1	4,675,806	06/1987	Uchida	364	200	
	AC1	4,722,049	01/1988	Lahti	364	200	
	AD1	4,807,115	02/1989	Torng	364	200	
	AE1	5,230,068	07/1993	Van Dyke *et al.*	395	375	
	AF1	5,442,757	08/1995	McFarland *et al.*	395	375	
	AG1	5,768,575	06/1998	McFarland *et al.*	395	569	03/13/1995
	AH1						
	AI1						
	AJ1						
	AK1						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	1	Smith *et al.*, "Implementation of Precise Interrupts in Pipelined Processors," *Proceedings of the 12th Annual International Symposium on Computer Architecture*, June 1985, pp. 36-44.
	AS	1	Wedig, R.G., Detection of Concurrency In Directly Executed Language Instruction Streams, (Dissertation), June 1982, pp. 1-179.
	AT	1	Agerwala *et al.*, "High Performance Reduced Instruction Set Processors," IBM Research Division, March 31, 1987, pp. 1-61.
	AU	1	Gross *et al.*, "Optimizing Delayed Branches," *Proceedings of the 5th Annual Workshop on Microprogramming*, October 5-7, 1982, pp. 114-120.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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	AA2						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL2						Yes No
	AM2						Yes No
	AN2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	2	Tjaden *et al.*, "Representation of Concurrency with Ordering Matrices," *IEEE Trans. On Computers*, Vol. C-22, No. 8, August 1973, pp. 752-761.
	AS	2	Tjaden, Representation and Detection of Concurrency Using Ordering Matrices, (Dissertation), 1972, pp. 1-199.
	AT	2	Foster *et al.*, "Percolation of Code to Enhance Parallel Dispatching and Execution," *IEEE Trans. On Computers*, December 1971, pp. 1411-1415.
	AU	2	Thornton, J.E., Design of a Computer: The Control Data 6600, Control Data Corporation, 1970, pp. 58-140.

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	AA3						
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FOREIGN PATENT DOCUMENTS

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	AL3						Yes No
	AM3						Yes No
	AN3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	3	Weiss *et al.*, "Instruction Issue Logic in Pipelined Supercomputers," Reprinted from *IEEE Trans. on Computers*, Vol. C-33, No. 11, November 1984, pp. 1013-1022.
	AS	3	Tomasulo, R.M., "An Efficient Algorithm for Exploiting Multiple Arithmetic Units," *IBM Journal*, Vol. 11, January 1967, pp. 25-33.
	AT	3	Tjaden *et al.*, "Detection and Parallel Execution of Independent Instructions," *IEEE Trans. On Computers*, Vol. C-19, No. 10, October 1970, pp. 889-895.
	AU	3	Pleszkun *et al.*, "The Performance Potential of Multiple Functional Unit Processors," *Proceedings of the 15th Annual Symposium on Computer Architecture*, June 1988, pp. 37-44.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA4						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL4						Yes No
	AM4						Yes No
	AN4						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	4	Pleszkun *et al.*, "WISQ: A Restartable Architecture Using Queues," *Proceedings of the 14th International Symposium on Computer Architecture*, June 1987, pp. 290-299.
	AS	4	Hwu *et al.*, "Checkpoint Repair for High-Peformance Out-of-Order Execution Machines," *IEEE Trans. On Computers*, Vol. C-36, No. 12, December 1987, pp. 1496-1514.
	AT	4	Jouppi *et al.*, "Available Instruction-Level Parallelism for Superscalar and Superpipelined Machines," *Proceedings of the 3rd International Conference on Architectural Support for Programming Languages and Operating Systems*, April 1989, pp. 272-282.
	AU	4	Hwu *et al.*, "Exploiting Parallel Microprocessor Microarchitectures with a Compiler Code Generator," *Proceedings of the 15th Annual Symposium on Computer Architecture*, June 1988, pp. 45-53.

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	AA5						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL5						Yes No
	AM5						Yes No
	AN5						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	5	Colwell *et al.*, "A VLIW Architecture for a Trace Scheduling Compiler," *Proceedings of the 2nd International Conference on Architectural Support for Programming Languages and Operating Systems*, October 1987, pp. 180-192.
	AS	5	Uht, A.K., "An Efficient Hardware Algorithm to Extract Concurrency From General-Purpose Code," *Proceedings of the 19th Annual Hawaii International Conference on System Sciences*, 1986, pp. 41-50.
	AT	5	Charlesworth, A.E., "An Approach to Scientific Array Processing: The Architectural Design of the AP-120B/FPS-164 Family," *Computer*, Vol. 14, September 1981, pp. 18-27.
	AU	5	Acosta, Ramón D. *et al.*, "An Instruction Issuing Approach to Enhancing Performance in Multiple Functional Unit Processors," *IEEE Transactions On Computers*, Vol. C-35, No. 9, September 1986, pp. 815-828.

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	AA6						
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	AL6						Yes No
	AM6						Yes No
	AN6						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	6	Johnson, William M., Super-Scalar Processor Design, (Dissertation), Copyright 1989, 134 pages.
	AS	6	Smith, M.D. *et al.*, "Boosting Beyond Static Scheduling in a Superscalar Processor," *IEEE*, 1990, pp. 344-354.
	AT	6	Murakami, K. *et al.*, "SIMP (Single Instruction stream/Multiple instruction Pipelining): A Novel High-Speed Single-Processor Architecture," *ACM*, 1989, pp. 78-85.
	AU	6	Jouppi, N.P., "The Nonuniform Distribution of Instruction-Level and Machine Parallelism and Its Effect on Performance," *IEEE Transactions on Computers*, Vol. 38, No. 12, December 1989, pp. 1645-1658.

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	AA7						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL7						Yes No
	AM7						Yes No
	AN7						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	Z	Horst, R.W. *et al.*, "Multiple Instruction Issue in the NonStop Cyclone Processor," *IEEE*, 1990, pp. 216-226.
	AS	Z	Goodman, J.R. and Hsu, W., "Code Scheduling and Register Allocation in Large Basic Blocks," *ACM*, 1988, pp. 442-452.
	AT	Z	Lam, M.S., "Instruction Scheduling For Superscalar Architectures," *Annu. Rev. Comput. Sci.*, Vol. 4, 1990, pp. 173-201.
	AU	Z	Aiken, A. and Nicolau, A., "Perfect Pipelining: A New Loop Parallelization Technique*," pp. 221-235.

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	AA8						
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	AL8						Yes No
	AM8						Yes No
	AN8						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	8	Jouppi, N.H., "Integration and Packaging Plateaus of Processor Performance," *IEEE*, 1989, pp. 229-232.
	AS	8	Groves, R.D. and Oehler, R., "An IBM Second Generation RISC Processor Architecture," *IEEE*, 1989, pp. 134-137.
	AT	8	
	AU	8	

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